

FIG. 2

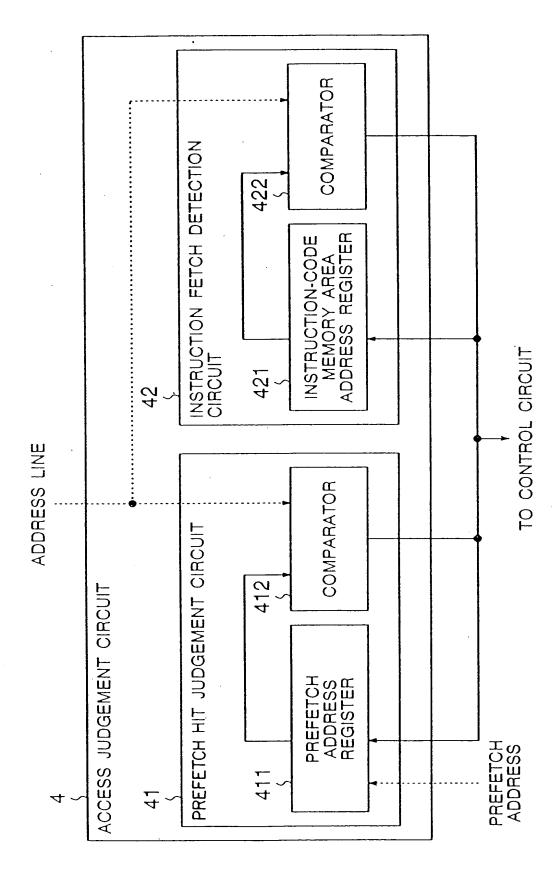
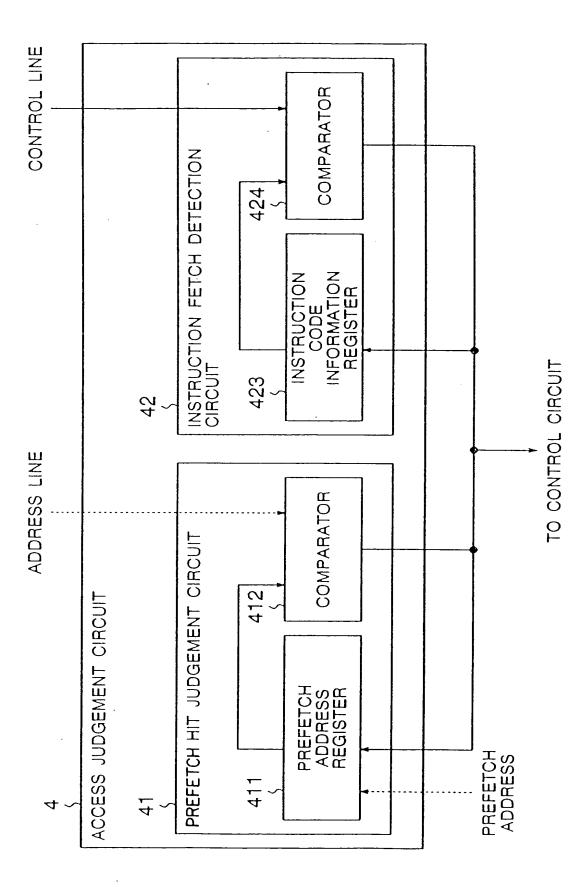


FIG. 3



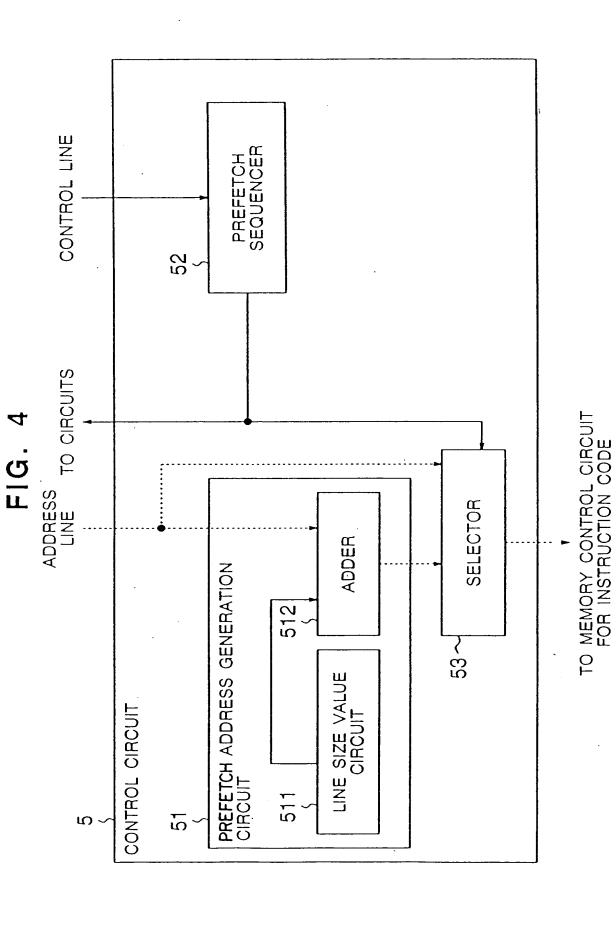
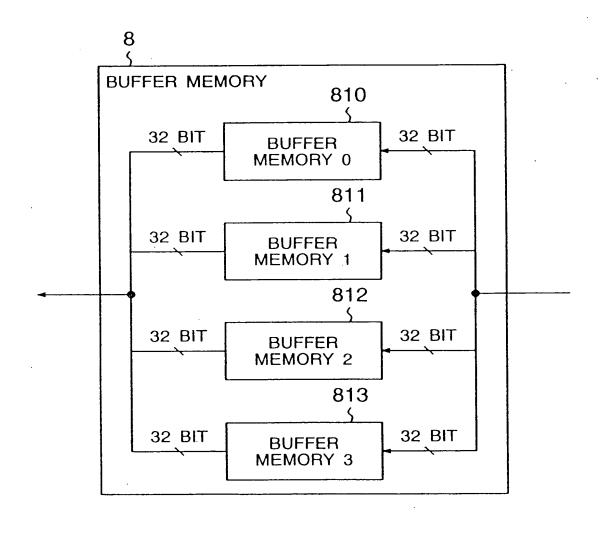
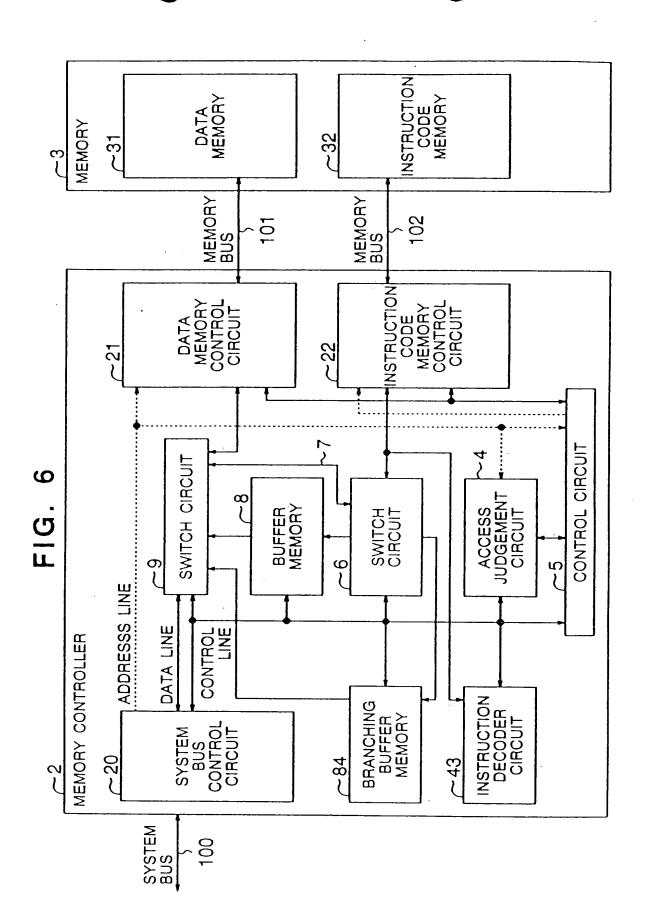


FIG. 5





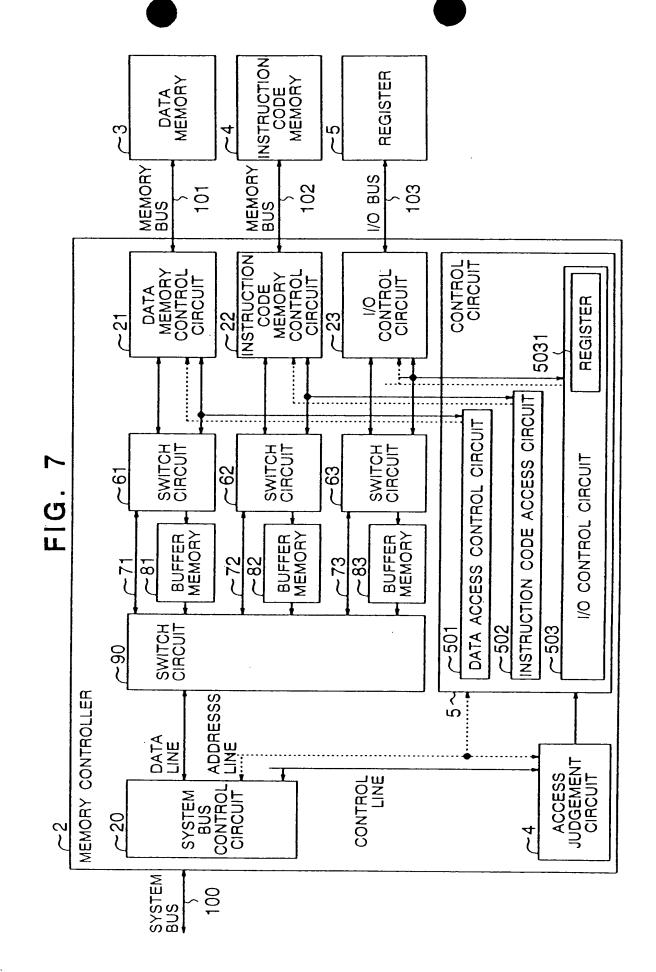


FIG. 8 **START** 201 **READ ACCESS** NO TO INSTRUCTION CODE AREA? 204 YES 202 TRANSFER INSTRUCTION CODE NO PREFETCH HIT? FROM MEMORY TO PROCESSOR VIA DIRECT PATH 203 YES START TRANSFER CLEAR BUFFER MEMORY OF INSTRUCTION CODE FROM BUFFER TO PROCESSOR 205 -206 ISSUE INSTRUCTION TO TRANSFER INSTRUCTION CODE OF NEXT ADDRESS FROM MEMORY TO BUFFER OF CONTROLLER BY AMOUNT CORRESPONDING TO ONE ACCESS SIZE -207 SET FETCH ADDRESS REGISTER

FIG. 9 **START** 211 **READ ACCESS** NO TO INSTRUCTION CODE AREA? 214 YES 212 **TRANSFER** INSTRUCTION CODE NO PREFETCH HIT? FROM MEMORY TO PROCESSOR VIA DIRECT PATH 213 YES START TRANSFER CLEAR BUFFER MEMORY OF INSTRUCTION CODE FROM BUFFER TO PROCESSOR 215 -216 SET FETCH ADDRESS REGISTER -217 RESIDUAL PREFETCH DATA IN BUFFER NO **CORRESPONDS** TO ONE LINE OR LESS? YES **ISSUE INSTRUCTION** -218 TO TRANSFER DATA OF CONTINUOUS ADDRESSES FROM MEMORY TO BUFFER OF CONTROLLER UNTIL BUFFER FULL

FIG. 10

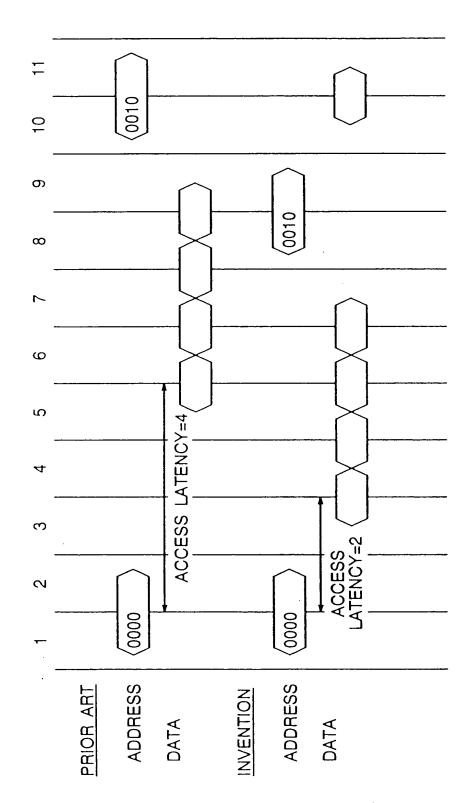
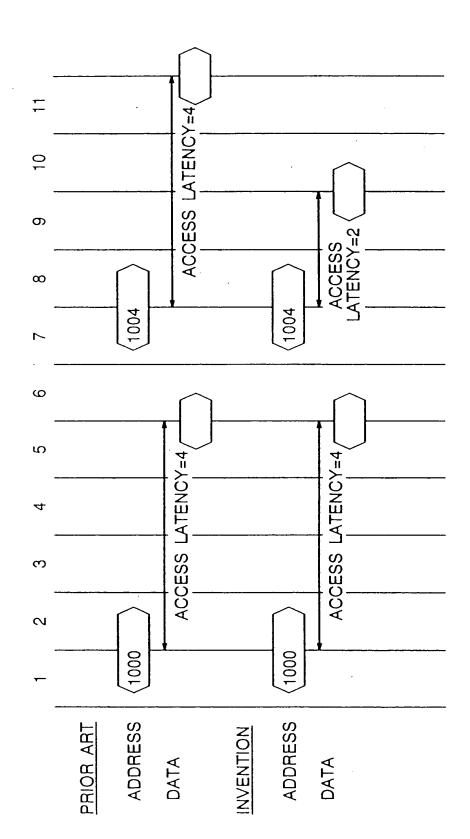


FIG. 11



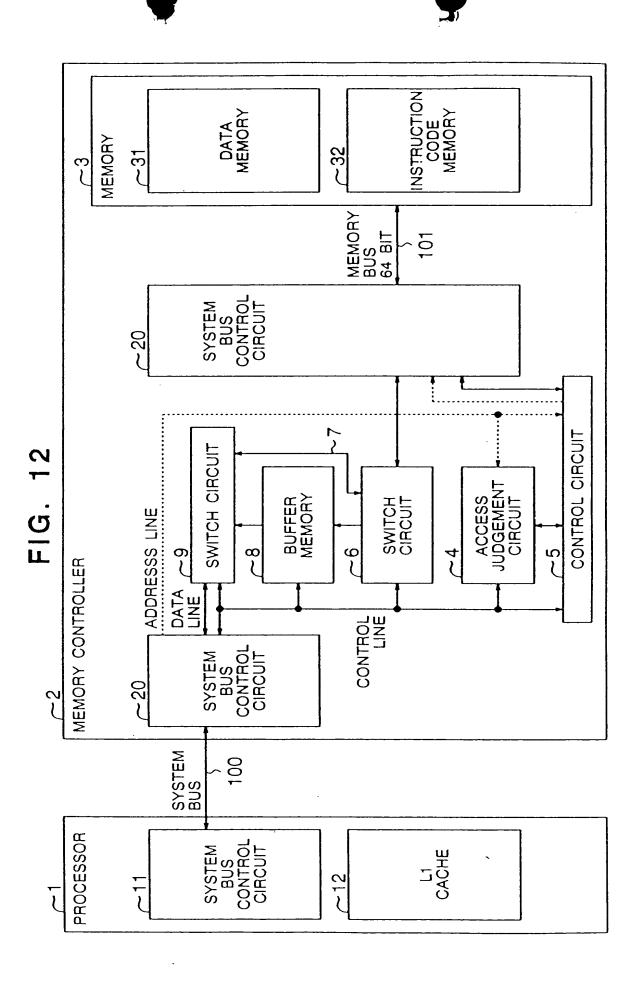




FIG. 13

